CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

1. An integrated circuit including an embedded memory and a built-in self-test arrangement including

means for storing test instructions including means for receiving test instructions provided from an external tester,

means for generating default test instructions, and

means for supplying said default test instructions to said means for storing test instructions.

2. An integrated circuit as recited in claim 1, wherein said means for generating default test instructions includes an initialization storage means.

3. An integrated circuit as recited in claim 2, wherein said initialization storage means is a storage initialization module.

4. An integrated circuit as recited in claim 1, further including

means for activating said means for generating said default test instructions responsive to an absence of test instructions from an external tester.

5. An integrated circuit as recited in claim 1, further including

means for controlling a test operation, wherein said means for controlling a test operation includes means for supplying a control signal to an instruction storage controller and further includes said means for storing said test instructions.

6. An integrated circuit as received in claim 5, further including

means for activating said means for generating said default test instructions when only said control signal is supplied to said instruction storage controller.

7. An integrated circuit as recited in claim 1, wherein said means for generating default test instructions includes a memory for storing said default test instructions.

8. An electronic system including an integrated circuit having a built-in self-test arrangement therein, said integrated circuit including

means for storing test instructions including means for receiving test instructions provided from an external tester,

means for generating default test instructions, and

means for supplying said default test instructions to said means for storing test instructions.

9. A system as recited in claim 8, wherein said means for generating default test instructions includes an initialization storage means.

10. A system as recited in claim 9, wherein said initialization storage means is a storage initialization module.

11. A system as recited in claim 8, further including

means for activating said means for generating said default test instructions responsive to an absence of test instructions from an external tester.

12. A system as recited in claim 8, further including

means for controlling a test operation, wherein said means for controlling a test operation includes means for supplying a control signal to an instruction storage controller and further includes said means for storing said test instructions.

13. A system as recited in claim 12, further including

means for activating said means for generating said default test instructions when only said control signal is supplied to said instruction storage controller.

14. A system as recited in claim 12, wherein said control signal is supplied from an external tester.

15. A system as recited in claim 12, wherein said control signal is supplied from within said system.

16. A system as recited in claim 8, wherein said means for generating default test instructions includes a memory for storing said default test instructions.

17. A method of performing system level tests on an electronic system including an integrated circuit having a built-in self-test (BIST) arrangement therein for performing manufacturing level and board level testing and including means for storing a test algorithm, said method comprising steps of

providing a system level test algorithm from said BIST arrangement,

transferring said system level test algorithm to said means for storing a test algorithm in said BIST arrangement, and

operating said BIST arrangement using said system level test algorithm.